# A 16-channel Digital TDC Chip

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**Abstract**

A 16-channel digital TDC chip has been built for the DIRC Cerenkov counter of the BaBar experiment at the SLAC B-factory (Stanford, USA). The binning is 0.5 ns and the full-scale 32 microseconds. The data driven architecture integrates channel buffering and selective readout of data falling within a programmable time window. The linearity is better than 80 ps rms on 90% of the production parts.

## 1 Context

The Detector of Internally Reflected Cerenkov photons (DIRC) detector [1] in the BaBar experiment measures the time of arrival of Cerenkov photons produced in 144 quartz bars on a wall of 11,000 photomultiplier tubes. In order to reconstruct the ring image, the machine induced background noise has to be rejected. The main part of this background is not in time with the event, and a sub-nanosecond measurement of the photons time of arrival is required.

### *1.1 Noise in the DIRC*

The noise in the DIRC due to the PMTs themselves is estimated to 1 kHz, the PEP II machine noise is estimated to 30 kHz including a safety factor of ten; for an average $b\bar{b}$ event, 5.7 primary tracks hit the DIRC and produce each 33 photoelectrons to which must be added six extra hits from background generated by these tracks. An equivalent number of background photons of the order of 200 is generated by secondary interactions between the event tracks and the detector (mostly Compton scattering in the quartz). The Level 1 (L1)

trigger is built from Drift Chamber, Calorimeter, and Muons Detector primitives. Its latency is 12 microseconds, with an uncertainty of one microsecond. Raw data are stored locally in the TDC chips during the L1 trigger latency. A local selection in this chip is furthermore performed so that only data occuring within a one microsecond window around the trigger are sent to the Data Acquisition System.

## 2 TDC requirements

The Time to Digital Converter (TDC) chip integrates the following functions:

- 0.5 ns binning with 250 ps rms precision.
- 32 $\mu$s full-scale and 32 ns double-hit resolution.
- Simultaneous Read and Write operations.
- Maximum rates:
  - Single channel rates of ten times the nominal background: 100 kHz
  - Maximum random rate on 16 channels simultaneouly: 10 kHz
- Data within a programmable time window before a readout request available at any time.
  - latency from 100 ns to 16 $\mu$s (eight bits).
  - window size from 100 ns to 2 $\mu$s (five bits).
- Bit pattern flagging the overloads during the trigger window.
- Power less than 200 mW at 100 kHz average input rate.

## 3 TDC architecture

The DIRC digital TDC chip (Figure 2) receives 16 outputs from two 8-channel zero-crossing discriminators timed with the single photo-electrons responses of the DIRC detector PMTs. On any Level 1 trigger (L1) occurence, digitized time data associated to this trigger are transferred to a Multi-Event Buffer (MEB) and stay until a readout request (Readout Strobe) originated in the central control and timing system occurs. A block diagram of the chip is shown Figure 1. Within a 59.5 MHz input clock period, a fine time measurement on 5 bits is achieved with voltage-controlled digital delay lines synchronized on the clock period using a calibration channel that generates a reference voltage, to compensate for temperatures, supplies, and process delays variations. This calibration is fully transparent to the TDC operations.

A synchronous counter covers the 11 higher order bits. In order to allow data-driven operations and asynchronous readout occuring at any trigger time during BaBar runs, sixteen dual port FIFOs reaceive data from the TDC section.

Three level of buffering in FIFO memories allow to store data in time with an incoming trigger, and make them available for readout. This feature allows to reduce by a factor of 10 the amount of data to be read from the DIRC detector. Each FIFO overload during a trigger window is reported at the end of each data block as a sixteen bit pattern. A maximum average channel input rate of 600 kHz is accepted, as far as there are less than four input hits on the same channel within a window of one microsecond, and less than 96 inputs on any of the 16 channels within one trigger latency.

The chip is manufactured by ATMEL-ES2, using a 0.8 microns CMOS double-metal process.

### *3.1 Time measurement*

The TDC section integrates one 60 MHz counter, 16 digital delay lines with 32 taps of 500 ps delay each, one calibration channel made of a delay line identical to the measuring channel, locked on the clock using two analog controls stored in the gate capacitors of transistors controlling the delays of the 32 identical stages, and a time offset.

These analog controls are common to all channels, assuming a good process uniformity within the chip. The uniformity had been measured on previous TDC chips designs using the same technology [2] [3].

An incoming signal latches the counter in a 11-bit register. It is also propagated through the delay line. The next clock positive edge latches the state of the delay line in a 32-bit register, the result being binary encoded to five bits. Extra cells on each side of the delay line allow to lock the total delay and offset on the clock period.

### *3.2 Phase locking*

A state machine sequences the calibration process, sending clock pulses as inputs, tuning the channel to give back zero and full-scale digitizations alternately. This process is basically convergent, and no loss of lock can be observed. Therefore, it is not monitored. Calibration is internally activated at low rate, giving the best linearity results.

### *3.3 Selective Readout*

A block diagram of the selective readout is shown Figure 3. The TDC section is sensitive to any positive edge applied to the inputs. Datum is stored for one microsecond at more in a four-deep channel FIFO. There is one FIFO for each channel, they are emptied by a continuous read process at 30 MHz that extracts the oldest datum among the sixteen channel FIFOs outputs (actually the oldest from each FIFO), and transfers it to a 32-deep latency FIFO (FIFOl), shared by all channels, where it stays until the minimum L1 latency (actually the latency minus half the resolution). It is then transfered to a 32-deep FIFO where it stays until the maximum trigger latency (latency plus half the resolution). During that stage, a L1 accept is followed by a readout command that empties this FIFO and outputs a data packet whose header is the L1 accept time (on 11 bits), followed by the time words ordered by 32 ns slices, and terminated by a trailer flagging input FIFO overloads. These informations have been buffered in a dedicated FIFO with the associated time, and processed in the same way as the time data during the selective readout process.

The readout process is sequenced at 30 MHz, and can be managed within the time before another L1 accept comes (1.5 $\mu$s). When data is readout, the selective readout process filling the output FIFO is still working. There is no deadtime associated.

The fast sort algorithm [4] is based on a slicing in time windows. From two adjacent channels, two bits from time words (bit 10 and 9) belonging to a window of 256 ns are input to eight comparators, the oldest data being compared two by two in the same way, until the last. There are 128 time windows. Therefore, fifteen two-bit comparators in three stages are used. The width of 256 ns is fixed by the response time of the comparator tree, and the maximum input occupancy. It allows to use small and fast comparators with 18 ns response time. The tree returns the address of the oldest time datum for transfer to the latency FIFO.

### *3.4 Latency and Output FIFO management*

This section sends data from the Latency FIFO to the Output FIFO if they are in time with a just incoming trigger (Figure 4). The current time is first subtracted from the time data, if the result is more or equal to the sum of the latency and half the resolution, the time data is sent after the trigger latency minus half the trigger resolution to the Output FIFO, provided it is not full. If no trigger has come after the latency plus half the resolution, data is lost.

The writing rate can be up to 1/32 ns at that stage.

### *3.5 Deadtime*

These three levels of buffering have been implemented in order to cope with the required single channel rates of ten times the nominal background of 10 kHz per channel, and the simultaneous maximum random rate on 16 channels of 10 kHz. The transfer from each TDC section to each channel FIFO is immediate. With the same assumption for the transfer from the channel FIFO to the latency FIFO, the dead time can be estimated for various latency FIFO depths. FIFO depths of 4 and 32 have been implemented for the channel and the latency FIFO respectively, according to the simulation results, leading to a minimum dead time less than 0.1 % as required for input rates of 100 kHz.

### *3.6 Performance tests*

#### *3.6.1 Test Bench*

Test benches have been set up at each stage of the chip development. First versions were used for checking prototypes linearity and overall functionalities. The last test bench aimed to fully test the production parts within a few minutes. Tests were also performed on the Front-end cards of the DIRC with actual PMTs signals as inputs. The production test bench makes use of a Pentium PC, a LeCroy 9210 precision pulser, and a dedicated printed circuit board housing a hardwired sequencer, digital interfaces to the PC and the chip socket.

#### *3.6.2 Selective readout*

The selective readout process has been checked by sending an input synchronous with the trigger window while a set of PMTs generated random noise.

#### *3.6.3 Linearity*

The histogram of the bin widths has been built by sending random inputs. On channel 14 and 15, the last bin has been found up to two times too wide. It is understood as a layout effect although all TDC channels have been replicated identical and the delay lines control voltages do not deliver any static current. A coarse counter slipping by one clock tick was observed on a few chips (3.3

% of 896 TDC channels when all channels are fired together at the same time. Due to the last bin width, some chips needed to be calibrated on 31 bins instead of 32. Then, the number of faulty channels is reduced to 0.3%. On the production, 792 chips were calibrated on 32 bins and 420 chips on 31 bins.

### *3.6.4 Deadtime*

A good agreement is found between simulated and measured deadtime, both for random events on the sixteen channels, and synchronous events (Figure 4).

### *3.6.5 Production for the DIRC*

All the chips have been successfully tested by the manufacturer using an 8k test-vector file in order to check the digital functions. A dedicated LabView test software was used on a PC Pentium (233 MHz) in order to test each chip in 2 to 3 minutes. The global performances observed on the production chips were similar to those of the preproduction chips although the general behaviour is slightly better. Over 1250 chips, 38 were not working properly due to faults in the analog sections, diagnosed using an extra 10k test vectors that were not accepted by the manufacturer standard flow. As another selection criterium, it was decided to reject chips with a bin 31 larger than the others by 20%, or chips with bin 0 or/and 1 smaller by more than 60% than the average (those introducing coarse counter slips), having selected the best calibration scheme. 805 chips satisfied these criteria.

### *3.6.6 Tests in the context of the DIRC Electronics.*

The selected chips have been tested on the twelve DIRC sectors after the PMTs have been mounted and fully wired. In total, 805 chips satisfied the selection criteria. The distribution of the delay lines differential linearity was peaked at 35 *ps* when the chips were calibrated on 32 bins (Figure 5). The average differential linearity on all chips and all channels is 73 *ps*. This corresponds to a time resolution of about 196 *ps* including the binning error.

## 4 Conclusion

This digital TDC chip is a building-block of the Front-End electronics [5] for the Detector of Internally Reflected Cerenkov light of the BaBar experiment at SLAC (Stanford, USA). Twelve hundred parts have now been fabricated

and tested with a very good yield. Time resolution and input rate capabilities have been measured within the initial requirements. The selective readout process reduces by a factor of ten the amount of data to be read for the DIRC detector.

## References


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