Electronics commands for the DIRC calibration

DIRC *electronics and calibration groups*

1 Introduction

At the DIRC electronics PDR review in London (June 1996), it was deemed necessary to precise the electronics aspects of the DIRC calibration. This document is an attempt to respond to that request. It should also help nailing down more specifically the specifications of the Fast Control System.

The calibration system is described in details in the DIRC note #25[1]. Early considerations on calibration mainly from the online point of view can be found in DIRC note #16[2]. We recall the main features of the system in section 2. We list next (section 3) the working decisions that have been made to date. We expect them to be frozen in Dresden. The following sections describe in turn each type of calibration run we anticipate for BABAR and their motivations. For each instance, the configuration control commands and the run time commands are distinguished. Please refer to ref.[3] for an exhaustive accounting of the DIRC local commands. We anticipate the actual calibration procedures from 1998 on will evolve from the a priori description we give in this paper. We have also included for completeness some description of procedures that will be enacted for the frontend electronics commissionning and a list of configuration control commands that will have to be done prior a normal data taking run. Finally, a summary of the points which address the specifications of the Fast Control System is given.

2 Overview of the DIRC calibration system

The DIRC calibration encompasses detector calibration mainly done using a light pulser device and electronics calibration. Moreover, while data taking the PMT working points are constantly monitored by sampling the charge of some hits in the events. As described in [1], 12 LEDs strategically located on the standoff box illuminate the DIRC PMTs. There is one LED per sector which is associated to the sector in front of it but which also lights tubes on the 2 adjacent sectors. Each LED is fed by a dedicated pulser which receives a trigger pulse from the DCC in the frontend electronics. The frontend electronics also comprise the DFBs which have to be ready to accept the signals from the hit PMTs. Electronics calibration is performed using fake PMT signals at the entrance of the DFBs. For the commissioning of the frontend electronics provision is made to send bit patterns to key locations.

3 Working decisions

- Immediate readout of calibration events, i.e no provision for stacking data from many calibration events on the DFB before DAQ readout.

- *Charge multiplexing.* The above implies dropping the fancy multiplexing scheme that had been invented for charge measurements where, among the hit tubes in a calibration event, priority is given to one which has not been recently hit to be connected to the ADC.

  Two multiplexing modes thus remain. One can direct to the ADC either the pulse of a selected PMT (channel select or encoder mode) or that of the first PMT among those hit (multiplexing mode). Dropping the fancy scheme has a price on the time needed to complete a calibration run. Part of this time can be overcome by looping on the static mask registers of the DFB (minor loop in the online language).

- DFB *timing gate* is hardwired instead of settable[1]. This is the delay of the CALSTROBE signal when it fires the sample/hold circuit for LED runs in *pedestal mode* where the charge is measured independantly of the output of the discriminators in the analog chip.

- The reference PMTs which were considered to guarantee the stablity in yield and timing of the light sources have been dropped.

- The existing pulser from Saclay is the baseline choice. It delivers high frequency light pulses (up to 100 kHz) with a timing stability better than needed (jitter and width both less than 1 ns) and ultrastable light output (see [1]) once set.

- Correlation between time and amplitude measurements for photoelectrons will not be done.

- *LED trigger.* Each LED is triggered by a NIM pulse out of the associated DCC. There are 3 gangs of 4 LEDS illuminating sectors at right angles. The 4 diodes in a gang are fired simultaneously. A $\simeq$ 100 ns delay is used between successive gangs sufficient to allow matching a given hit to the LED which emitted the photon by time. The time at which a DCC sends the NIM pulse is settable between 0.5 and 512 ns by a 10 bit register. The pulse leading edge is defined with 0.1 ns precision.

4 Different types of runs

As indicated in ref.[1] there will be LED runs to measure the PMT gains, the time offsets (t_0) of every channel and monitor the photoelectron detection efficiency drifts. In the *self gated* mode described in section 5.1 which will be performed routinely on a daily basis, the data flows exactly as during the experiment i.e. only pulses above threshold have their charge recorded. Pedestal runs (sect. 5.2) will be performed on a daily basis to monitor the noise. Obviously the sample and hold for charge measurement has to fire on a CALSTROBE independantly of the output of the discriminators on the analog chips. This

[1] The DFB group 1 register called *Calibration timing register* can be removed and all commands which involve it are useless.

defines *pedestal mode*. Note that LED data can also be acquired in *pedestal mode* to study the noise and signals in time with a LED pulse. Electronics calibration runs using fake PMT analog pulses (sect. 5.3) will be extensively performed while commissionning the boards.

Frontend electronics commissionning is also the time when digital tests will require specific configurations of the boards (sect. 6). When data taking only a minimal set of checks of the vital parts on the DFB and on the DCC should be done at begin run (sect. 7). The last 2 run types are not calibration runs strictly speaking. That means they do not (necessarily) require sending CALSTROBE commands repeatedly.

Under various circumstances (shutdown, debugging phases, etc.) more extensive calibration runs or commissionning procedures will be performed. They are basically extensions of the types that have been outlined above.

What follows is a rather dry technical description of commands. A guide for those is ref.[3]. DIRC local commands are used for configuring the frontend electronics. These commands comprise a 5-bit opcode with the MSB (bit-4) set, a 5-bit (sub)address and optional data. The last 2 bits of the opcode select a group of registers (0=readout setup registers; 1= calibration registers; 2= internal DFB tests; 3= reserved). The BABAR global commands L1, ReadEvent and Calibration Strobe (CALSTROBE) are used during the actual calibration runs. All runs have a basic (most internal) sequence where CALSTROBE, L1 and ReadEvent are issued in a row for a prescribed number of events. This sequence could be nested into a more or less complex loop structure.

The configuration commands are presented below in tables. The contents of all registers not appearing in the tables are assumed to be irrelevant for the considered run type, unless otherwise stated.

5 Calibration runs

5.1 LED run (*self gated*)

The purpose of this routine run is to check the gains, the t_0's and the efficiency drifts by recording the time and the amplitude for some 10^3 hits for every channel. The time and charge measurements are performed exactly as during a normal data taking run. In particular, the ADC is gated by the appropriate discriminator in the analog chip.

5.1.1 Configuration

Refer to table 1.

5.1.2 Run

The basic run would contain no loop. To get more precision on the t_0 measurements, a loop on the fine DCC delay will be done[2]. The minimum time for the

[2] A run with a loop is split in successive run sequences separated by configuration procedures where one or more parameters are changed. In the case of interest, the DCC timings would

Configure	opcode (hexa)	subad	# data bits	data meaning
DCC delay	19	8	10	(10) default setting (*)
DCC enable LED	19	9	1	(1)=1 LED firing enabled
DFB calib. mode	19	0	7	(2)=3 all channels active (2)=1 signal origin=LED (1)=0 ADC gated by discri (1)=0 no meaning anymore (1)=0 ADC enabled
DFB Threshold DAC	18	0-F	8	(8)=Threshold value
DFB ADC MUX mode	18	11	7	(1)=0 encoder mode (preferred) =1 otherwise followed by (6)= address of the wanted channel
DFB TDC latency/resol.	18	16	16	(8)= upper edge of trigger window (8)= lower edge
DFB ADC ch. enable(*)	18	12-15	16	bit pattern =1 for enabled channel
DFB TDC ch. enable	18	16-19	16	bit pattern =1 for enabled channel

Table 1: Configuration commands for LED runs. Possible loops are indicated by (*). Reducing the width of the trigger window could be useful for this and other calibration runs. The last 2 commands could be used to disable high rate channels when real time is short.

most basic run has been estimated to be of the order of one minute[1]. This estimate has been computed assuming all LEDs fire on each CALSTROBE.

5.2 Pedestal run

A pedestal run is used to record the noise spectra of the PMTs and check the pesdestal values. The ADC is gated by CALSTROBE.

5.2.1 Configuration

See table 2.

5.2.2 Run

A pedestal run requires a loop on the channel addressed by the ADC. After each loop, the configuration change may involve modifications in masking, although this is not probable.

Notice that **LED calibration in pedestal mode** is possible. The signal paths on the DFB are as just described. The configuration is that of table 2 except for the subcommands (given in table 1) which activate the LEDs (DCC) and prepare the DFB to accept signals originating from LED. Recording the amplitude at a fixed time with respect to CALSTROBE independantly of the

be changed.

Configure	opcode (hexa)	subad	# data bits	data meaning
DCC disable LED	19	9	1	(1)=0 LED firing disabled
DFB calib. mode	19	0	7	(2)=3 all channels active
				(2)=0 signal origin=none
				(1)=1 ADC gated by CALSTROBE
				(1)=0 no meaning anymore
				(1)=0 ADC enabled
DFB Threshold DAC	18	0-F	8	(8)=Threshold value
DFB ADC MUX mode (*)	18	11	7	(1)=1 channel select followed by
				(6)= address of the wanted channel
DFB TDC latency/resol.	18	16	16	(8)= upper edge of trigger window
				(8)= lower edge
DFB ADC ch. enable	18	12-15	16	bit pattern =1 for enabled channel

Table 2: Configuration commands for a pedestal run. A loop (64 steps) on the command tagged by (*) is required. The last command could be used to disable channels if necessary.

discriminators outputs enables to study the setting of the threshold in the analog chip in a non destructive way.

5.3 Electronics calibration (analog pulsing)

5.3.1 Configuration

This type of run is used to fake PMT signals at will at the entrance of the analog chips in order to calibrate the electronics, study crosstalk, charge measurements, etc. The local commands are detailed in table 3.

5.3.2 Run

Loops on the pulsed channels (odd/even) to study crosstalk, and on threshold values to vary the PMTs working points will be implemented.

6 Electronics commissionning (digital patterns)

The pattern generator on the DFB is used to send words to various places on the digital part of the DFB. The configuration commands are given in table 4.

The DFB internal tests are performed with the BABAR protocol local commands as explained in ref.[3]. The use of global commands in such commissionning runs has yet to be defined.

Configure	opcode (hexa)	subad	# data bits	data meaning
DFB calib. mode	19	0	7	(2)=1 or 2 odd/even(*) (2)=2 signal origin=DFB pulse gen. (1)=0 or 1 ADC gated by discri or not (1)=0 no meaning anymore (1)=0 ADC enabled
DFB calib. DAC	19	1	12	(12)=DAC value(*)
DFB Threshold DAC	18	0-F	8	(8)=Threshold value(*)
DFB ADC MUX mode	18	11	7	(1)=1 channel select followed by (6)= address of the wanted channel
DFB TDC latency/resol.	18	16	16	(8)= upper edge of trigger window (8)= lower edge
DFB ADC ch. enable	18	12-15	16	bit pattern =1 for enabled channel
DFB TDC ch. enable	18	16-19	16	bit pattern =1 for enabled channel

Table 3: Configuration commands for an analog electronics calibration run. Possible loops on parameters flagged by (*). The last 2 commands could be used to disable channels.

Configure	opcode (hexa)	subad	# data bits	data meaning
DFB calib. mode	19	0	7	(2)=any (2)=3 signal origin=DFB pattern gen. (1)=any (1)=any (1)=1 Disable ADC
DFB TDC ch. enable	18	16-19	16	bit pattern =1 for enabled channel
DFB internal tests				see ref.[3]

Table 4: Configuration commands for electronics commissionning using bit patterns. Writing (and reading) at various locations in the DFB is accomplished by DIRC local commands with hexadecimal opcodes 1D and 1A (and 15 to 10) for various subaddresses. Single word and block transfer data transmission are implemented. The last command could be used to disable channels.

7 Normal data taking configuration

At the beginning of a normal data taking run brief tests on the most vital parts on the DCC and DFB are to be done to make sure the DIRC electronics is up and running. Appropriate digital tests have to be devised and incorporated in the sequence of local commands to be executed at the configuration phase. the relevant local commands have yet to be defined.

In order to record the charge of hit PMTs the ADC should be set up with multiplexing on.

The local commands are shown in table 5.

Configure	opcode (hexa)	subad	# data bits	data meaning
DFB calib. mode	19	0	7	(2)=any (2)=0 not a calibration (1)=0 ADC gated by discris (1)=0 no meaning anymore (1)=0 ADC enabled
DFB Threshold DAC	18	0-F	8	(8)=Threshold value
DFB ADC MUX mode	18	11	1	(1)=0 multiplex
DFB TDC latency/resol.	18	16	16	(8)= upper edge of trigger window (8)= lower edge
DFB ADC ch. enable	18	12-15	16	bit pattern =1 for enabled channel
DFB TDC ch. enable	18	16-19	16	bit pattern =1 for enabled channel
DCC test status	?	?	?	tbd
DFB test status	?	?	?	tbd

Table 5: Configuration commands for normal data taking run.

8 Implications for the Fast Control System

The frequency of the global commands sequences in the run phase is assumed to be 10 kHz for all run types except for pedestal runs. This number matches the DAQ processor speed. If the processor technology progresses enough, the limit ($\simeq$ 30 KHz) could come from the bandwidth between frontend electronics and DAQ. A higher frequency (100 kHz) would be welcome for pedestal runs but is not necessary. Our request to the FCS would be that it can generate trigger frequencies up to 30 kHz. Notice that all rates mentioned above imply that the calibration constants are extracted from data within the DAQ readout crate, so that the output rate towards the level3 farm remains within specs (2 kHz).

References

[1] P. Bourgeois et al., Report on the DIRC LED Calibration System, DIRC note # 25, (26 Feb. 1996).

[2] D.N. Brown and G. Oxoby, Proposal for a DAQ and Online Test Stand for the DIRC, DIRC note #16, (14 November 1995).

[3] DIRC Electronics Group at Orsay, The DIRC subsysem commands, Specifications for the DIRC Front-end Board, (20 June 1996).