1 DIRC Digital TDC Chip Reference.

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Introduction

The DIRC digital TDC chip is a building block of the DIRC Front-End electronics. [1] [2]. It receives 16 outputs from two 8-channel Zero-crossing discriminators (Analog chip) timed with the single photo-electrons responses of the DIRC detector PMTs. On any Level 1 trigger (L1 accept) occurence, digitized time data associated to this trigger are transferred to an external Multi-Event Buffer.

1 Requirements.

The DIRC Digital TDC chip has to meet the following requirements [3]:

- 0.5 ns binning with 1/2 LSB rms precision.
- 32 μs full-scale.
- 32 ns double-hit resolution.
- 59.5 MHz reference clock.
- Simultaneous Read and Write operations. Two reads minimum spacing: 2μs.
- Input capability:
  - Above 100 kHz on any channel.
  - 10 kHz with simultaneous hits on every channel.
- Selection of data within a programmable time window available at any time for readout.
  - Latency between 64 ns and 16,284 μs (eight bits).
  - Window size between 64 ns and 1,984 μs (five bits).
- Bit pattern flagging the channel FIFOs overloads during the trigger window.
- Channel disabling of the noisy channels between 500 kHz and 8 MHz.
- Bit pattern flagging either FIFO overload or channel disable during the associated window.
- Power under 100 mW at 100 kHz average input rate.
- Temperature range: 15-40 Celsius.

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2 Overall description

A block diagram of the chip is shown Fig 1. Within a 59.5 MHz input clock period, a fine time measurement on 5 bits is achieved using voltage-controlled digital delay lines synchronized on the clock period using a calibration channel generating a reference voltage, to compensate for temperatures, supplies, and process delays variations. This calibration is fully transparent to the TDC operations.

A synchronous counter covers the 11 higher order bits.

In order to allow data-driven operations and asynchronous readout occuring at any trigger time during BaBar runs, sixteen dual port FIFOs allow data to be written from the TDC section.

Three level of buffering in FIFO memories allow to sort data in time with an incoming trigger, and make them available for readout. This feature allows to reduce by a factor of 10 the amount of data to be read from the DIRC detector. Each FIFO overload or channel disabling during a trigger window is reported at the end of each data block as a sixteen bit pattern.

A maximum average channel input rate of 600 kHz is accepted, as far as there are less than 4 input hits on the same channel within a window of one microsecond, and less than 96 on any of the 16 channels within one trigger latency. Input double pulse resolution is 32 ns.

The chip is manufactured by ES2, using a 0.7 microns Dual Metal CMOS process.

2 Time digitization

The TDC section integrates one 60 MHz counter, 16 digital delay lines with 32 taps of 500-ps delay each, a calibration channel made of a delay line identical to the measuring , locked on the clock using two analog controls stored in the gate capacitors of nMOS transistors controlling the delays of the 32 identical stages, and a time offset.

These analog controls are common to all channels, assuming a good process uniformity within the chip, measured on previous TDC chips designs using the same technology .

An incoming signal latches the counter state in a 11-bit register, and is propagated in the delay line. The next clock positive edge latches the state of the delay line in a 32-bit register, the result being binary encoded to five bits. Extra cells on each side of the delay line allow to lock the total delay and offset on the clock period.

The delay lines, the synchronization mechanism between the clock and the time inputs, the 60 MHz counter, the charge pump used as phase feedback have been implemented as full-custom designs, simulated with Spice, before and after layout.

A state machine sequences the calibration process that can be activated using an input pin. The end of that process which takes a few microseconds in total, activates an output

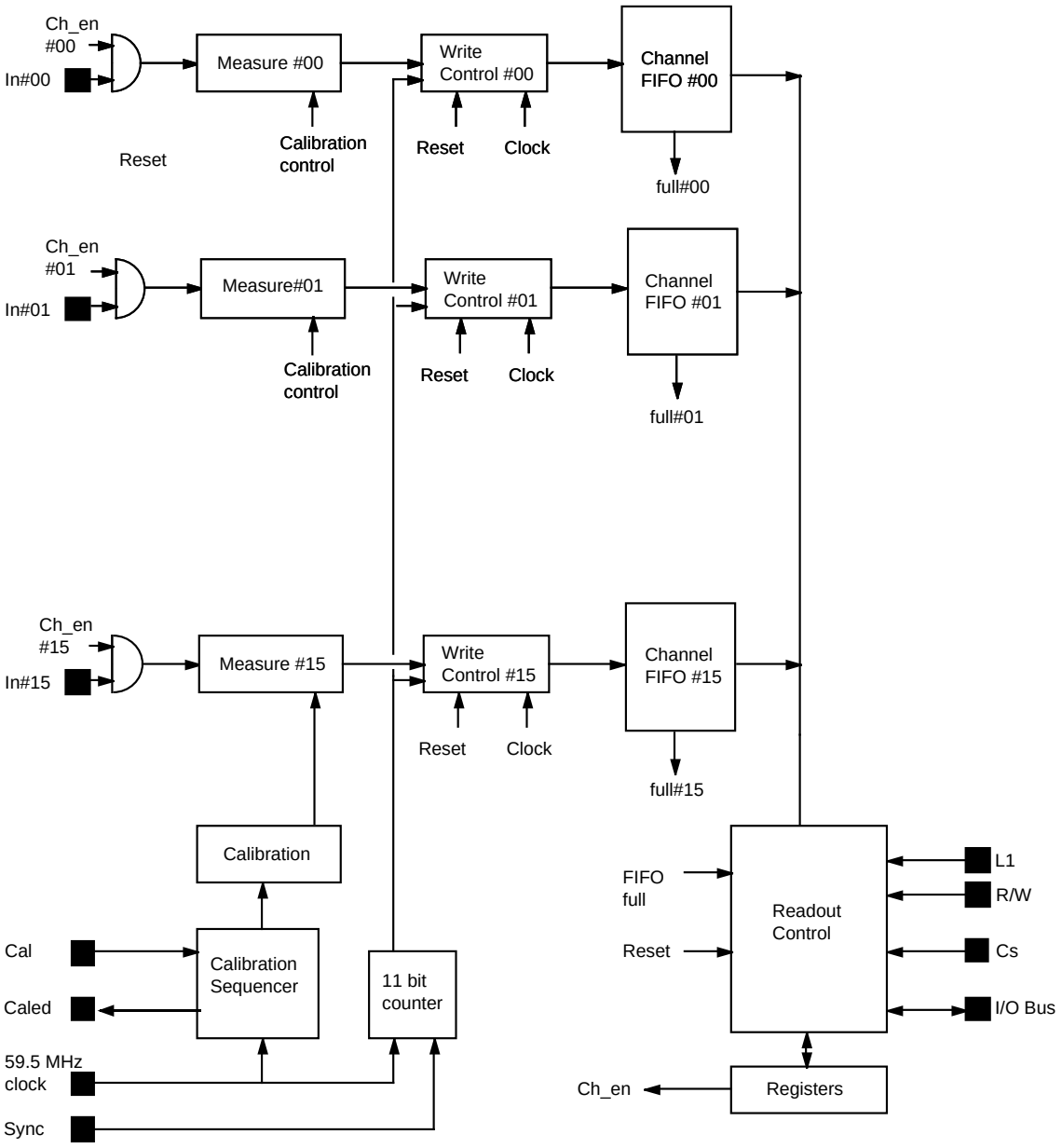

Figure 1: DIRC Digital TDC Chip Block Diagram.

signal. Calibration has been found stable for minutes, allowing to keep the chip free of any other switchings than the necessary measurements, giving the best linearity results.

3 Selective Readout

A block diagram of the selective readout (Selective readout) is shown Fig. 2. The TDC section is sensitive to any positive edge applied to the inputs. Datum is stored for one μs at more in a four-deep channel FIFO. There is one FIFO for each channel, they are emptied by a continuous read process at 30 MHz, that sorts the oldest datum among the sixteen channel FIFOs outputs (actually the oldest from each FIFO), and transfers it to a 32 deep latency FIFO (FIFOl), shared by all channels, where it stays until the minimum L1 latency (actually the latency minus half the resolution).

It is then transferred to a 32 deep FIFO (FIFOo) where it stays until the maximum trigger latency (latency plus half the resolution). During that stage, a L1 accept is followed by a readout command that empties this FIFO and outputs a data packet whose header is the L1 accept time (on 11 bits), followed by the time words ordered by 32 ns slices, and terminated by a trailer flagging some input FIFO overload, or channels that have been self-disabled due to input overload. These informations have been buffered in a dedicated FIFO with the associated time, and processed in the same way as the time data during the selective readout process.

The readout process is sequenced at 30 MHz, and can be managed within the time before another L1 accept comes (1.5 μs). When data is readout, the selective readout process filling the output FIFO is still working. There is no deadtime associated.

4 Channel Disabling

A noisy PMT channel, or an oscillating discriminator can lock the TDC selective readout process by filling the latency FIFO. In that case, good data coming from other channels will be lost. A dynamic disabling process counts the input hits during a given time slice, programmable between 256 and 4,096 clock periods (4.3 and 68.81 μs, by steps of 256 clock periods (4.3 μs) using a four-bit register. If this count exceeds 32, the channel is disabled until the next time slice. Corresponding input frequencies are 500 kHz and 8 MHz. If a channel is disabled, and L1 occurs in the associated time window, a bit is set in the 16-bit pattern status word appended as a trailer to the data packet that is to be readout.

Independently, channels can be individually enabled or disabled using a dedicated register masking the corresponding inputs.

5 Registers

Four registers are used to control the device.

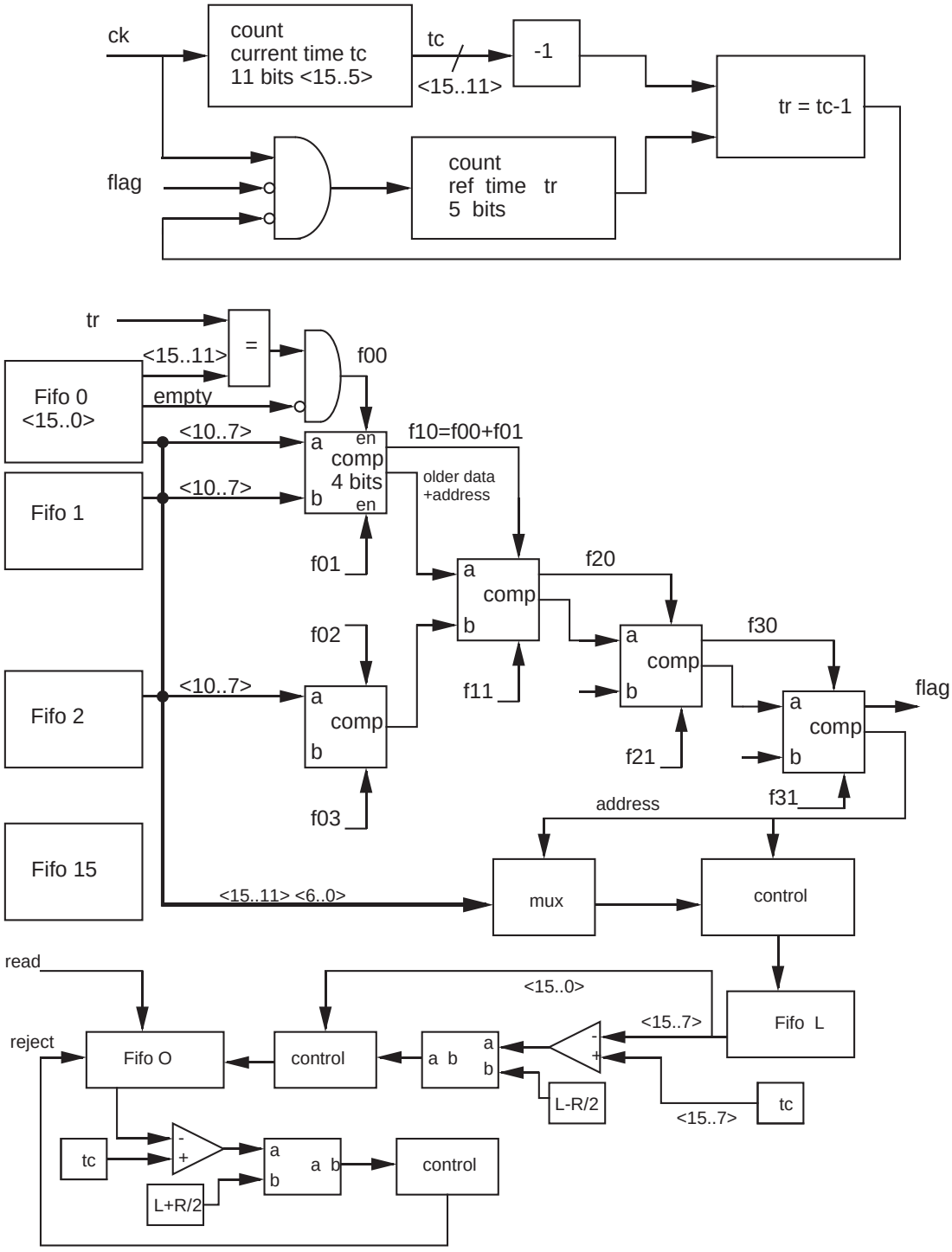

Figure 2: Selective readout process block diagram.

- Latency and Resolution are specified using two separate sets of two 16-bits registers, used for the selective readout process, and for the generation of the status word.
- A 16-bit register can be accessed for Channel Enabling or Disabling.
- The channel disabling window is specified in a 5-bit register.

Any register can be read back. (Annex 1).

6 Tests

The chip mixes three design styles, with their specific test strategy.

- Full-custom.

  Most of the TDC section including the 17 fine time delay lines, the 16-bit counter, the channel FIFOs, the calibration charge pump, the synchronizing logic between the clock and the inputs have been implemented in full-custom.

  The test of this section cannot be supported and results granted by any automated test equipment from a Silicon manufacturer, since it implies control of subnanosecond delays. However, a good fraction of the circuitry can be tested just propagating an edge from the inputs through the delay lines.

  This full-custom area is 30% of the chip.

- Macrocells.

  The latency, resolution, and status FIFOs have been implemented using a generator provided in the ES2 Cadence design kit.

  A Verilog model, symbol and hardware black box, is generated, including the Built In Self Test (BIST) circuitry, and test vectors.

- Standard Cells.

  The registers, bus and I/O control, state machines and selective readout have been designed using ES2 standard cells, most having been synthesized using the Synopsys software tool. They are tested using a scan path test mode where flip-flops have been added automatically by the synthesis tool on critical nodes, and can be written in sequence. The result of a stimulation is available on the data outputs when this test mode is selected.

7 I/Os Description

- S(0:15) Start inputs. 16 independent TTL inputs.

  Any positive pulse of more than 5 ns duration applied to these pins results in a time digitization of the rising edge with respect to the clock.

- Bs(0:1) Bus Select. Two TTL inputs.

  These bits, combined with Bist and D(21:20) as input, select the function of the multiplexed inputs/outputs D(21:0). This 22 bit port is used for data access, register read and write, tests input and output, scan test access as follows:

  All data (registers or time data) are true logic, MSB left.

  Bs = 00 D(21:0) = Data output.

  Bs = 01 D(21:0) = Parallel access for register read or write. See below Bist.

  Bs = 10 D(21:0) = Tests. See below Bist.

  Bs = 11 D(21:0) = Selects scan test mode, combined with Bist.

  In this mode, 310 bit long scan test vectors are input sequentially on the Ci pin. They are output in the same order on Xxo. Results of a given test is available on D(17:0), with D(21:20) = 01 as input. See below Bist, Xxo.

- D(15:0) 16 Input/Outputs TTL in, CMOS out.

  Bs = 00 Data outputs 15-0.

  Bs = 01 Parallel access bus for register Read and Write.

  Bs = 10 Test data output 15-0.

- D(19:16) Four CMOS outputs.

  Bs = 00 Data outputs 19-16.

  Bs = 10 Test data output 19-16.

- D(21:20) 2 Input/Outputs TTL in, CMOS out.

  Function selection for multiplexed inputs combined with Bs and Bist, when used as inputs.

  Bist selects as follows:

  Bist = 0:

  Bs selects as follows:

  Bs = 00. Digital TDC chip running mode.

  Bs = 01. Register Write and Read access.

  D(21:20) as inputs select as follows:

  D(21:20) = 00.

  Trigger Latency and Resolution on 16 bits. Registers governing the selective readout process.

  8 bits: [Latency - (Resolution/2)-1] MSB first. 8 bits: [Latency + Resolution /2] MSB first.

Unit is four clock periods in ns. Values between 0 and 16 microsecond can be selected for Latency, 0 and 1984 ns for Resolution at 60 MHz clock operations.

D(21:20) = 01.

Trigger Latency and Resolution (L,R) on 16 bits. Second Word redundant with the first, used for Input FIFO Overload status bit pattern.

Format:

6 bits: [int[(L-[R/2] -2)/R] -1)] MSB first, 5 bits: L - (R/2) - R * [int[(L-[R/2] -2)/R] -1)] MSB first, 5 bits: (R -1) in four clock periods units (66.4ns at 60 MHz clock operations).

D(21:20) = 10.

Channel Enable Register. 16 bit pattern, active true.

D(21:20) = 11.

Channel Disable Window, Time Data Tests, Calibration Control. Channel Disable window controls the self-disabling capability of the chip. A channel is disabled if there is more than 32 input pulses during a window programmable between 3.84 microsecond and 61.44 microsecond at 60 MHz clock period. Channel is enabled in the next time window if less.

Format MSB first:

2 bits tests, 3 zeroes, 1 bit calibration control, 4 bits Channel Disable window, 8 zeroes.

The calibration control bit tunes the last bin of the interpolator for the chips where it is found too large due to the process spreads. Zero is the regular value (500 ps). Bs = 10. Test Mode.

D(21:20) as inputs select as follows:

D(21:20) = 00. Test Channel FIFOs section.

Rw = 0. Write: D(17:0) as test vector inputs.

Rw = 1. Read: D(17:0) as test vector outputs.

D(21:20) = 01. Test TDC section.

Rw = 0. Write: D(17:0) as test vector inputs.

Rw = 1. Read: D(17:0) as test vector outputs.

Bs = 10. Test Mode.

Bs = 11. Scan Test Mode.

Bist = 1:

D(21:20) as outputs. Bist test results (signature) of latency FIFO and output FIFO.

- Ck, TTL Input. Clock input.

  Frequency between 50 and 90 MHz can be used. Duty cycle between 40% and 60%.

- Rw, TTL Input. Read Write registers control.

  Selects Read or Write Registers. 0 = Write, 1 = Read. Data bus direction is set internally.

- Strb, TTL Input. Strobe for register access.

  Strobe used to write or read registers.

  Rw = 0. Write Register. Data should be stable at least half a clock period before strobe positive edge, maintened half a clock period afterwards.

  Rw = 1. Read Register. Data is enabled on the data bus at least half a clock period after strobe negative edge.

- L1, TTL Input. Trigger accept input.

  This input has to be synchronous with the clock, maintened high for one clock period starting on a falling edge. Trigger time associated to that period is internally latched on the clock leading edge. See Figure 3.

  Data falling in the selected time window are output synchronously with an internal 30 MHz clock cleared by Sync (See below). First data is Trigger time on 11 bits, available during the 30 MHz clock period following L1 assertion i.e. on the second or third 60 MHz clock period following L1 assertion, depending on the parity of the 60 MHz L1 assertion with respect to the internal 30 MHz clock. Time data follow at 30 MHz rate, until xxo that flags the output FIFO empty state goes low (see Xxo, and Figure 3.) Xxo goes low with L1, and high with the assertion of the last word to be output (trailer).

Data packet structure.

Two MSBs indicate whether the word is a header 10, data 00, or a trailer 11. First word is Trigger Time on 11 bits.

Format:

10, four zeroes, 11 time bits MSB left, five zeroes.

Time data within the trigger window follows.

Format:

00, four channel address bits MSB left, 16 time bits MSB left.

Last word is a channel FIFOs status bits trailer. Status bit pattern flags the occurence of a channel FIFO overload during the trigger time window. Format:

11, OR of the channel FIFO 16 bit pattern, 3 zeroes, 16 bit pattern (channel zero left).

- Sync, TTL Input. Clear Time Counter.

  This pin receives the Sync global command from the BaBar Fast Control and Timing System. Clears the 60 MHz time counter. Clock synchronous. Low during one 60 MHz period. Counter is cleared on the clocks rising edge. Coarse and fine time internally cleared on the clock rising edge. Trigger time is zero for that clock period. Clears also the 30 MHz internal 2-divider providing the 30 MHz clock.

- Cs, TTL Input. Chip Select.

  Chip Select. Active low. Sets the data bus output buffers in the high impedance state when high.

- Res0, TTL Input. Clear FIFO.

  Clear all FIFOs. Active low.

- Res1, TTL Input. Reset.

  Resets all, including registers. Active low.

- Ci, TTL Input. Multiplexed pin. Calibration input, scan test input.

  Bs selects as follow:

  Bs = 00. Calibration input. Triggers a calibration cycle. Used for Off-DIRC chip tests.

  Bs = 11. Scan test input. Used for off-DIRC chip tests.

- Co, CMOS Output. Calibration output.

  Flags a calibration cycle termination. Used for off-DIRC chip tests.

- Bist, CMOS Input.

  Built In Self Tests input for Latency and Output FIFOs. Active high. Triggers a Bist sequence resulting in a Bist signature output. Used for off-DIRC chip tests.

- Xxo, CMOS Output. Multiplexed pin. Strobe for output data, Scan Test output, Bist output.

  Bist as input selects as follows:

  Bist = 0:

  Bs selects as follows:

  Bs = 00: Strobe for output data. Two clock period long. Data to be latched on rising edge. See Figure 3.

  Bs = 10: Internal Synchronization test result. Used for off-DIRC chip tests.

  Bs = 11: Scan test output. Used for off-DIRC chip tests.

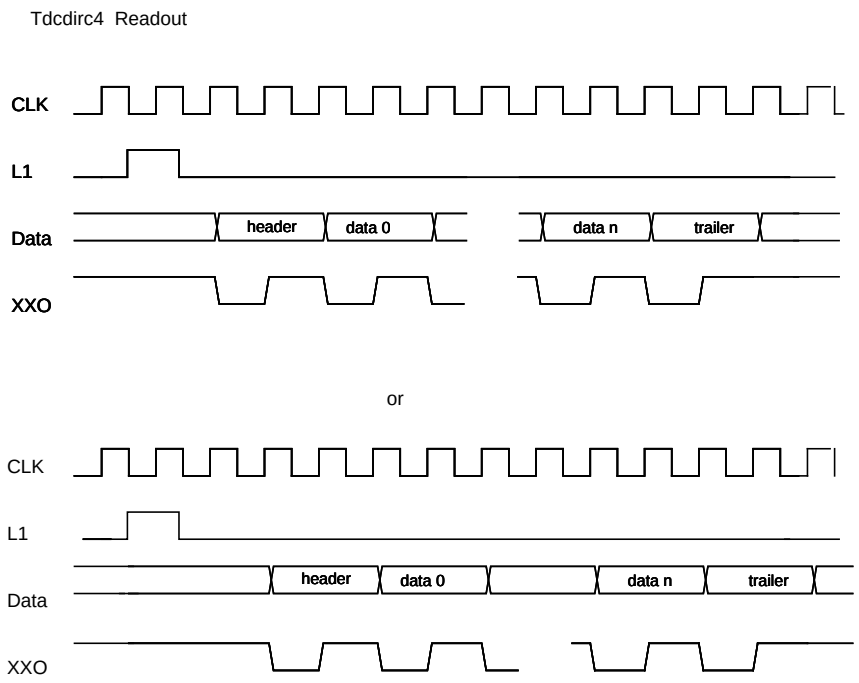

Figure 3: DIRC Digital TDC Chip Readout Sequence.

Bist = 1:

Channel FIFO Overload Bist tests signature output. Used for off-DIRC chip tests.

- Eight Vdd pins.
- Eight Ground pins.

8 Tests Benches.

Two test benches are used:

- A digital test-bench that makes use of:
  - A dedicated multi-layer printed circuit card,
  - Low voltage supplies,
  - A clock generator,
  - A MacIntosh computer running LabView,
  - A Digital I/O interface,
  - A dedicated test software that compares the outputs patterns with the predicted ones and pass the chip to the analog tests session or definitely rejects it.

- An analog tests bench that makes use of: - A dedicated multi-layer printed circuit card,
  - Two precision 9210 LeCroy IEEE 488 programmable pulsers,
  - Low voltage supplies,
  - A clock generator,
  - A MacIntosh computer running LabView,
  - A digital I/O interface,
  - A dedicated test software with provision for histogramming, automated time scans, diagnostics.

  The key measurements are:

  - Locking range,
  - Linearity within one clock period,
  - Linearity over several clock periods,
  - Underflows and overflows histograms,
  - Selective readout with simultaneous read and write,
  - Input capability,
  - Double-pulse resolution,
  - Self-disabling capability,
  - Data packet generation,
  - Crosstalk,
  - Power.

  A chip is definitely accepted after this test if it matches the requirements detailed in the first section.

9 Power.

The chip dissipates less than 100 mW at 100 kHz average input rate, and 2 kHz trigger rate, less than 10 mW if not activated.

10 Package.

The DIRC TDC chip is a packaged in a standard JLCC 68 pins package.

References.

-1 The BaBar DIRC Electronics Front-End Chain. The DIRC Electronics group. BaBar Note 395. October 1997.

-2 A 16-Channel, 500 Picosecond Resolution TDC Chip. Philippe Bailly, Jean-Francois Genat, Herve Lebbolo, Zhang Bo.
IEEE Nuclear Science Symposium, November 1996 Anaheim CA USA.

-3 DIRC Electronics Requirements. Writeup submitted to the PDRR, Paris, December 12th, 1995.

-4 A 500-ps resolution TDC chip for the DIRC at BaBar. Philippe Bailly, Jean-Francois Genat, Herve Lebbolo, Zhang Bo. 1997 Electronics for Particle Physics Conference at LeCroy, May 28-29, 1997 New-York USA.

-5 DIRC Digital TDC Prototype Chip Test Results. Philippe Bailly, Jean-Francois Genat, Herve Lebbolo, Zhang Bo. June 1997.

Documents 1, 3 and 5 are available on the Web from the BaBar Detector home page at http://www.slac.stanford.edu/BF/doc/www/bfHome.html through ELEC/DIRC/FDR.