DIRC TDC Prototype Chip Tests Results.

This report describes the tests results of the second prototype TDC chip designed at LPNHE Universites Paris 6 et 7 for the DIRC detector of BaBar. This chip is close to the DIRC Front-End Digital Chip pre-production version, presently under design. This chip has been sent to Europractice (IMEC Leuven, Belgium) in February 1996, and samples have been tested at LPNHE Paris.

1 TDC prototype chip functions.

The prototype chip whose bock diagram is shown in Fig 1 integrates the following functions:

- - 16 TDC channels, with:
  - 500 ps binning, 32 μs full scale,
  - 32 ns double hit resolution,
- - One transparent calibration channel,
- - 16 dual port channel FIFO's of 4 X 18 bits words each,
- - A selective readout of data in time with the L1 trigger including two 8 bits comparators and:
  - A 32 X 20 bits Trigger Latency FIFO,
  - A 16 X 20 bits Output FIFO,
- - A status FIFO for channel FIFOs overloads reports
- - A self-disable of noisy channels.

The next chip will be the DIRC Digital Chip pre-production version that includes a more efficient fast sort processor improving the input rate capability by a factor of 5 with respect to the present version, in order to cope with the Cherenkov radiation from muons crossing the water of the DIRC detector, triggering half the detector. It integrates also full control of the time data within the context of the DIRC Front-end Boards (DFBs).

2 Principle.

This TDC integrates basically one counter running at the clock frequency (this frequency will be 59.5 MHz during BaBar runs), 16 digital delay lines [1] with 32 taps of 500 ps delays, sixteen channel FIFO memories with simultaneous write access from timing section, and read access from the data output port, synchronous with the clock. One delay line channel

is used to calibrate the 16 delay lines of the active channels on the clock period, in order to compensate delays for supply, process and temperature variations.

Input signals are propagated in the delay lines whose state is latched in output encoder registers with the next incoming clock edge. The state of the counter is then transferred in the channel FIFO's, together with the registers content.

The calibration process is a phase locked loop device, that tunes the delay lines on the clock period using two analog controls stored in the gate capacitors of pMOS transistors controlling the delays of the 32 identical stages, and a time offset. These analog controls are common to all channels, assuming good process uniformity within the chip.

Each delay line is tuned using a few 500 ps underflow and overflow cells at each end of the delay lines, of unlikely use when the chip is calibrated. The calibration process tunes first the time offset, during cycles for which a clock edge is sent as a Start into the calibration channel delay line and used as a Stop to latch the delay line state, then the offset analog control voltage is adjusted with a small current step charging the gate capacitors of the concerned delay stages in the proper way, according to the previous result. When calibrated, the response of the delay line oscillates between underflow and bin zero at each cycle.

The gain of the delay line is tuned in the same way, as a clock edge is propagated in the delay line, and the following one latches the state, adjusting the gain voltage to get a response oscillating between bin 32 and overflow.

These two adjustments are cycled until convergence is reached. The process is activated at reset, or on an hardware request using a dedicated pin. An output pin is used to flag the convergence. Shorting the two pins results in locking the calibration process on the clock period, as a Phase Locked Loop device.

3 Implementation.

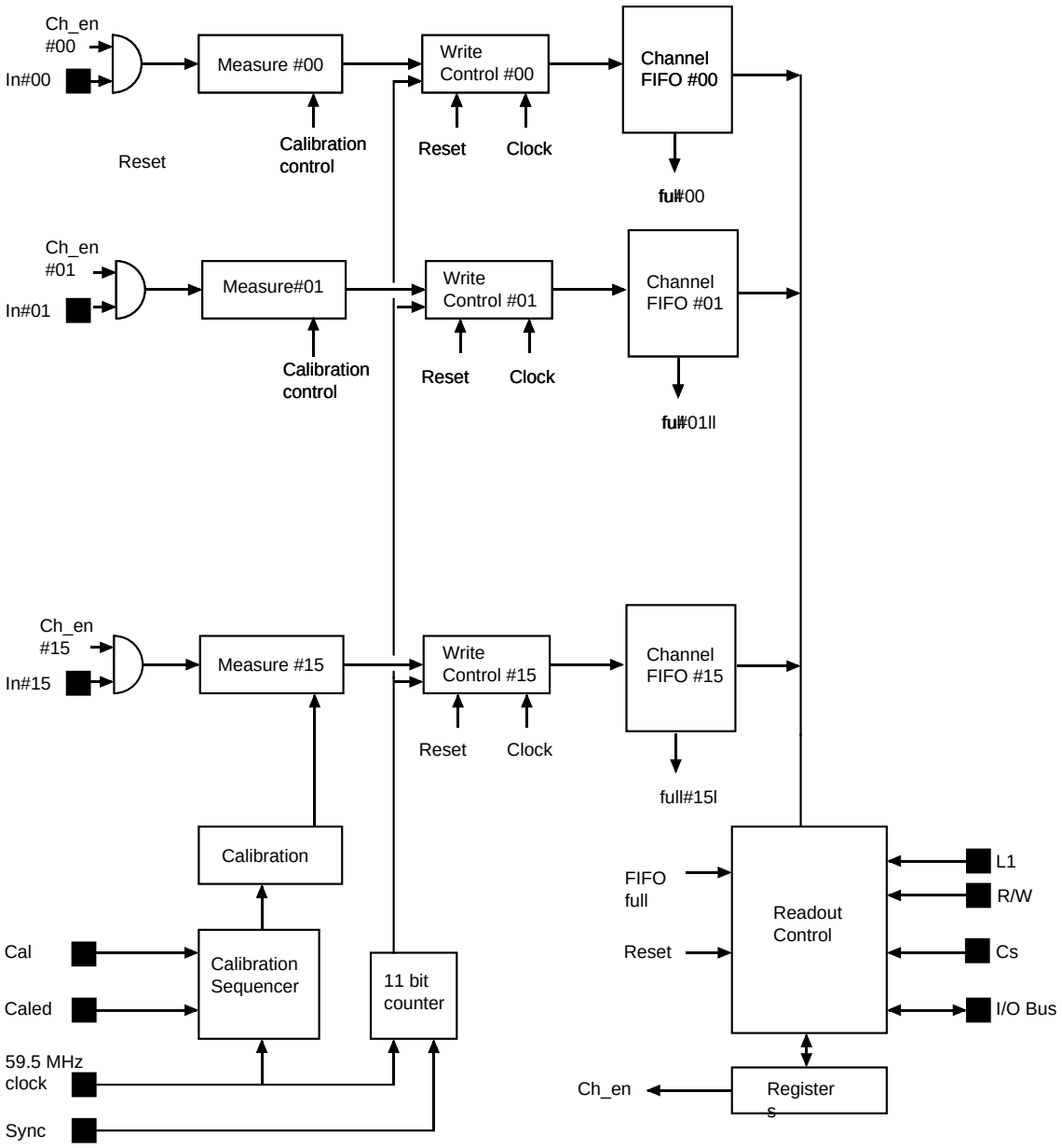
This chip has been designed using a 0.7 μ dual metal layer CMOS process from European Silicon Structures (ES2).

The delay lines, the synchronization mechanism between clock and time inputs, the 60 MHz counter, the charge pump used as a phase feedback have been implemented as full-custom design, and simulated with Spice, before and after layout. The full-custom editor, Preform developped at ENST Paris, interfaced to Cadence DFWII, has been used, allowing to go quickly from a stick layout description to the actual full-custom. Some connexions between analog blocks had to be done manually in order to minimize crosstalk, although the automated placing and routing tool from Cadence was used.

Digital design has been implemented using a high level description written in Verilog, synthesized into hardware with Synopsys, using standard cells provided by ES2.

The channel FIFO's have been implemented with a macrocell generator from ES2 on the prototype chip. On the Digital Chip, they are laid out as full-custom in order to save Silicon area.

A behavioural description of the delay lines and delay feedback has been written with Verilog, in order to allow a digital simulation of the full design, including the calibration process.



DIRC Digital Chip Block Diagram

Figure 1: Block Diagram.

4 Tests.

These first tests intended to check:

- Clock frequency range,
- Differential and integral linearity,
- Calibration spreads from channel to channel,
- Calibration stability and transparency,
- Selective readout and input capability,
- Crosstalk between channels,

5 Tests set-up.

In order to test the chips, a 4 layers PCB card has been designed, with 16 X 50 Ω time inputs, digital input/output ports and a readout sequencer allowing to digitize and read simultaneously, as well as to check the selective readout algorithm and the input capability.

It was connected to the following instruments:

- LeCroy 9210 fast pulser,
- IEEE488 I/O card,
- Philips PM5786 pulser as clock generator,
- Low voltage supplies.

The LeCroy pulser, the I/O card were under control of the LabView (National Instruments) software, running on a MacIntosh MacII Ci computer. A test software has been written, allowing to input various stimuli and use several readout modes, with provision for interactive test, histograms displays, statistics, and diagnostics.

6 Clock range.

The chip is clocked at 60 MHz. Simulations showed that a clock range between 40 and 80 MHz can be used, improved from 60-90 MHz measured on the first protoytpe.

The chips run as simulated between 45 up to 120 MHz for voltage supplies between 4.5V to 5.5V which is quite acceptable for the DIRC environment, since it allows to compensate for a wide range of temperature and process variations. The delays temperature coefficient is 0.4 % per Celsius degree.

7 Linearity.

The integral linearity for times between 30 and 100 μs is shown in Fig 2.The rms is 0.54 LSB. Other channels show similar performance.

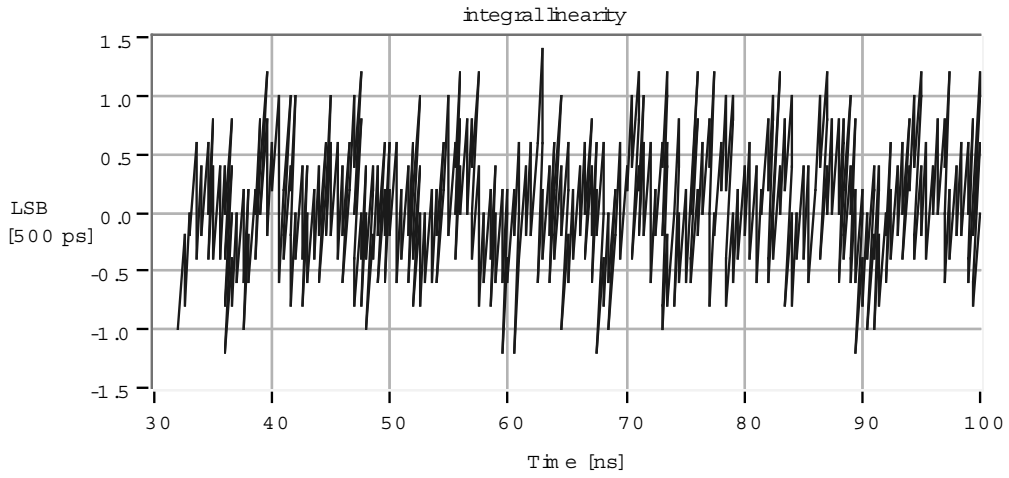


Figure 2: Integral linearity error between 30 and 100 μs. [LSB, time].

Another set of measurements was done within a clock period at 60 MHz, for each of the 16 inputs, pulsing with a given phase after the clock rising edge. This synchronous mode measures the silicon process spreads of the delay lines, and the mismatch of the two extreme bins, checking so the accuracy of the calibration mechanism.

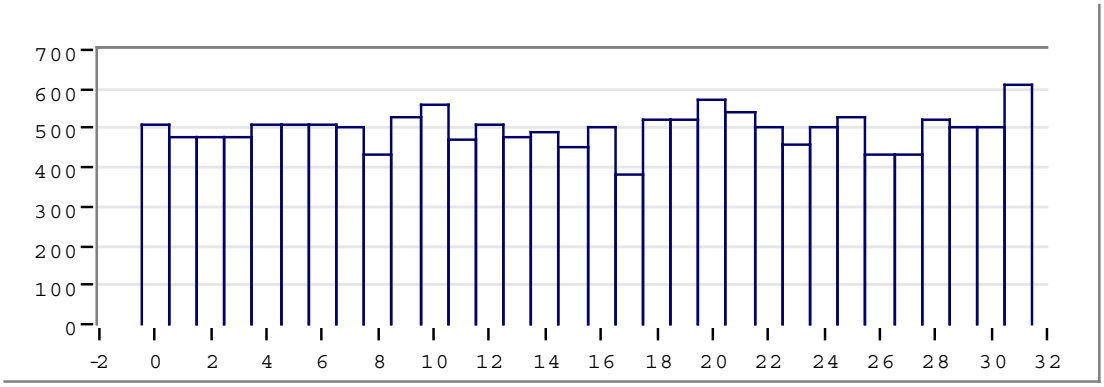


Figure 3: Differential linearity within one clock period. [picoseconds, channel number].

The delay line is actually built with 32 equal delay elements and 4 extra cells on each side, measuring time underflow and overflow with respect to the clock period. As the calibration is common to all channels, one expects some differences between the extreme bin sizes, from channel to channel. Underflow is measured before bin 0, overflow after bin 31.

Underflow measures the time mismatch for the cells before bin 0, overflow measures the time mismatch after propagation through the full chain, mismatch is expected larger by $\sqrt{32}$. The mismatch deduced from differential linearity measurement Fig 3 is 40 ps rms. One expects 250 ps on the full delay line. This is directly measured from Fig 6 (prototype 1) and Fig 7 (prototype 2). Fig 4 to Fig 7, show histograms of bin 0 and bin 31 for 16 channels of 8 measured chips. These two bins have been mixed with the underflow and overflow cells respectively in order to build true 16 bit time data. Bin 31 width indicates the difference from the average of the delay line length.

Bin zero is correct, as one expected from a delay equalisation between the calibration channel and the input channels, after prototype 1 understanding. Bin 31 is too large by 275 ps in average, with a spread of 145 ps rms. This is not yet understood, although some symmetry is found in the histogram of the 16 channels. This should be compared to the situation of the prototype 1 where bin 0 was too large by 210 ps in average, and bin 31 by 55 ps with a spread of 105 ps.

A problem arises for channels where bin 31 width exceeds 1ns. Then, it is possible that the delay line is latched after the last overflow cell, in a cell that is not encoded. The coded time is wrong by 16 ns in that case.

One has tried to slow down the clock edges to 2 ns (instead of 1ns in the previous results). Then, the delay lines are shifted in time such that bin 0 increases, and bin 31 decreases. The 16 ns error does not occur any more, and the chip works as expected.

Instead of making hazardeous layout changes to try to resize the delay line length, it has been decided to allow the calibration control to calibrate the total delay between 30 and 31, (instead of 31 and 32), in order to shift bin 31 by 500 ps. The delay line will be always latched on an encoded cell, the integral linearity being approximately kept within the same limits (error of 290ps in average for bin 31), but the counter value be correct in any case.

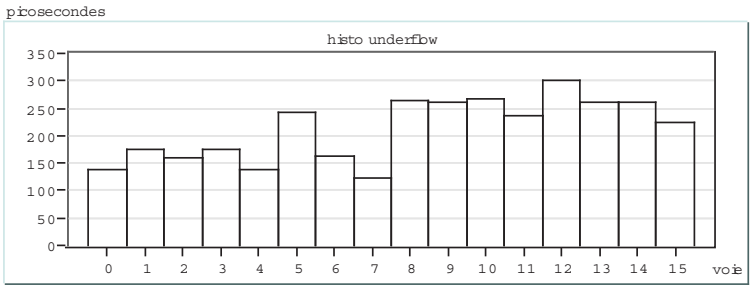


Figure 4: Histogram of bin 0 accumulated on 16 channels of 8 chips [picoseconds, channel number] Prototype 1.

8 Calibration stability.

Calibration of the delay lines on the clock has been found extremely stable, and no differences in measurements were found, for conversions with and without calibration running, except the 100 ps reduction of the overflow bin. The calibration cycle is 1 μs long, for this test, it was looped on

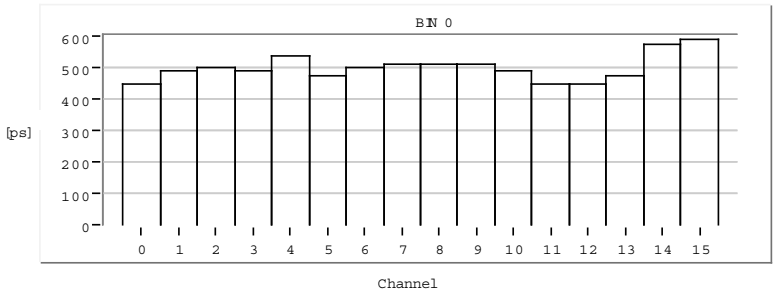


Figure 5: Histogram of bin 0 accumulated on 16 channels of 8 chips [picoseconds, channel number] Prototype 2.

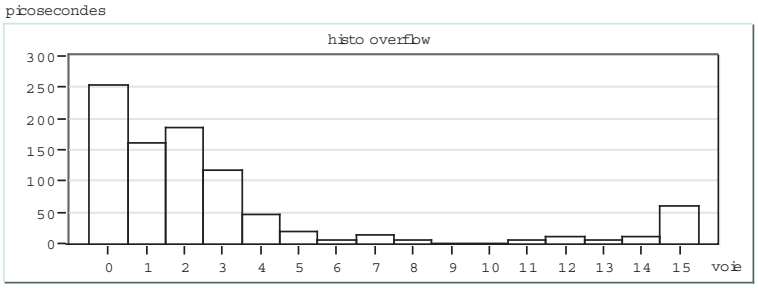


Figure 6: Histogram of bin 31 accumulated on 16 channels of 8 chips [picoseconds, channel number] Prototype 1.

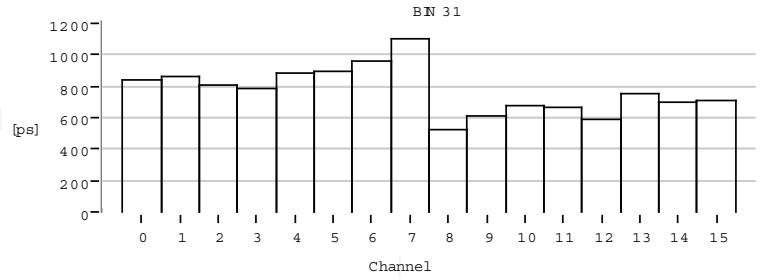


Figure 7: Histogram of bin 31 accumulated on 16 channels of 8 chips [picoseconds, channel number] Prototype 2.

itself at 1 MHz.

Calibration stability was checked over duration of several minutes, and neither drift nor noise was measured. However, the process will be activated periodically during BaBar runs. It is possible to loop the calibration on itself, resulting in a 1 MHz calibration frequency. This calibration is obviously completely transparent to the user.

9 Selective readout.

A selective readout of data falling within a programmable trigger window has been implemented. It is able to sort data from the input FIFOs in a 144 ns cycle (simulated and measured). All data presented here have been processed with this algorithm. However, in some cases, the implemented readout is not able to follow the input rate, when too much data are stored in the input FIFOs. There is no way to flag the situation. It was decided to implement another selective readout scheme in the digital preproduction chip (to be sent July 15th), where the sort will be done in 32 ns, and any saturation will be reported in the status word.

10 Crosstalk.

To be filled later. Results from prototype 1: 125 ps added in linearity rms when two adjacent channels are pulsed at the same time.

11 Yields

On 10 tested chips, eight work on 16 channels, one has some output bits stucked, and one channel from one chip does not work. A total yield of 50-60% is expected from production, for a targeted 250 ps rms precision on all channels.

Conclusion

The tests of this second prototype chip show that all problems of the first iteration are solved, except the exact tuning of the delay lines on the clock, that still need some improvement. An easy change in the digital control of the calibration will be made, keeping the full-custom design as it is, in order to get a satisfying yield from the production.